UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,995	11/13/2001	Chien-Ping Chung	JCLA7630	3462

23900 7590 03/28/2005

J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,995	CHUNG, CHIEN-PING	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 1/12/05. Currently claims 1-12 and 14-15 are pending.

Claim Rejections - 35 USC § 102

1. *Claims 6 and 8-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Klinger (US 6523071).*

Regarding claim 6, Klinger discloses at least one latching device, wherein said latching device has a triggering terminal and an output terminal, said triggering terminal couples with a configuration diagnostic signal lead of said IDE bus and said output terminal couples with a signal detection terminal of said detection device (e.g., col. 2, lines 59-67), where the latching device further includes a clear terminal such that said output terminal of said latching device is reset to a low potential when said clear terminal is triggered by a system reset signal (e.g., col. 6, lines 60-61).

Regarding claim 8, Klinger also discloses a general-purpose input/output (GPIO) controller (e.g., col. 6, lines 3-6).

Regarding claim 9, Klinger also discloses an integrated drive electronic (IDE) interface controller (e.g., col. 1, lines 30-36).

Regarding claim 10, Klinger also discloses an 80-pin connection or a 40-pin connection (e.g., col. 2, lines 43-46).

Regarding claim 11, Klinger also discloses the IDE bus is diagnosed as one having an 80-pin cable by said detection device if said output terminal of said latching device outputs a low potential to said signal detection terminal of said detection device (e.g., col. 6, lines 55-59).

Regarding claim 12, Klinger also discloses IDE bus is diagnosed as one having a 40-pin cable by said detection device if said output terminal of said latching device outputs a high potential to said signal detection terminal of said detection device (e.g., col. 6, lines 55-59).

Regarding claim 14, Klinger also discloses the device outputs a high potential when said triggering terminal of said latching device receives any signal variation (e.g., col. 6, lines 62-64).

Regarding claim 15, Klinger discloses a general purpose input/output (GPIO) controller having: a detection device having at least one of signal detection terminal for detecting IDE bus cable configuration (e.g., col. 3, lines 54-57); and a plurality of latching devices connected to said IDE bus cable and said detection device wherein each said latching device has a triggering terminal, a clear terminal and an output terminal, said triggering terminal coupling with a signal lead of said IDE bus (e.g., col. 6, lines 34-39); said clear terminal triggered by a system reset so that said output terminal of said latching device is reset to a low potential (e.g., col. 6, lines 60-61), and when said triggering terminal of said latching device receives any signal variation, said output terminal of said latching device outputs a high potential, wherein when said output terminal of said latching device outputs a low potential to said signal detection terminal

of said detection device, said IDE bus is diagnosed as having an 80-pin cable configuration, and when said output terminal of said latching device outputs a high potential, aid IDE bus is diagnosed as having a 40-pin cable configuration (e.g., col. 6, lines 57-60).

Claim Rejections - 35 USC § 103

2. *Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klinger in view of common digital design techniques, as evidenced by Rackley (US 5365122).*

Regarding claim 1, Klinger discloses a general-purpose input/output (GPIO) controller having at least one signal detection terminal for detecting IDE bus cable configuration (e.g., col. 5, lines 43-46); and a D-type flip-flop having a triggering terminal, a clear terminal, an output terminal and a data input terminal, wherein a triggering terminal couples with a signal pin of said IDE bus, said output terminal couples with said signal detection terminal of said GPIO controller, said clear terminal couples with a system reset terminal (e.g., col. 6, lines 60-61); wherein said clear terminal can be triggered by a system reset so that said output terminal of said D-type flip-flop is reset to a low potential (e.g., col. 6, lines 41-47), and when said triggering terminal of said D-type flip-flop receives any signal variation, said output terminal of said D-type flip-flop outputs a high potential; and when said output terminal of said D-type flip-flop outputs a low potential to said signal detection terminal of said GPIO controller,

said IDE bus is diagnosed as one having an 80-pin cable configuration, and when said output terminal of said D-type flip-flop outputs a high potential to said signal detection terminal, said IDE bus is diagnosed as having a 40-pin cable configuration (e.g., col. 7, lines 44-48). Klinger is expressly silent about the implementational details of using the triggering terminal of a D flip flop; however the Examiner takes Official Notice that it is widely known and practiced to use the clock input of a flip flop to sense signal variation. This is evidenced by Rackley who describes precisely this (e.g., Figure 1a). It would have been obvious to combine common digital design techniques with Klinger because the requirements of Klinger's sampling of a floating line, the details of which are expressly not disclosed, are commonly, simply, and advantageously solved by the well known technique of using a clock input on a flip flop. Therefore it would have been obvious to one of ordinary skill in the art to combine common practice with Klinger to obtain the claimed invention.

Regarding claim 2, Klinger also discloses wherein said latching device has a triggering terminal, a clear terminal and an output terminal, triggering terminal couples with a signal lead of said IDE bus and said output terminal couples with a signal detection terminal of said detection device (e.g., col. 6, lines 41-47); said clear terminal can be triggered by a system reset (e.g., col. 6, lines 60-61) so that said output terminal of said latching device is reset to a low potential, and when a triggering terminal of said latching device receives any signal variation, said output terminal of said latching device outputs a high potential; when said output terminal of said latching device outputs a low potential to a signal detection terminal of said detection device, said IDE bus is

diagnosed as having an 80-pin cable configuration, and when said output terminal of said D-type flip-flop outputs a high potential to said signal detection terminal, said IDE bus is diagnosed as having a 40-pin cable configuration (e.g., col. 7, lines 44-48). Klinger is expressly silent about the implementational details of using the triggering terminal of a D flip flop; however the Examiner takes Official Notice that it is widely known and practiced to use the clock input of a flip flop to sense signal variation. This is evidenced by Rackley who describes precisely this (e.g., Figure 1a). It would have been obvious to combine common digital design techniques with Klinger because the requirements of Klinger's sampling of a floating line, the details of which are expressly not disclosed, are commonly, simply, and advantageously solved by the well known technique of using a clock input on a flip flop. Therefore it would have been obvious to one of ordinary skill in the art to combine common practice with Klinger to obtain the claimed invention.

Regarding claim 3, Klinger also discloses D-type flip-flop having a clear terminal such that said clear terminal couples with a system reset terminal and said data input terminal couples with a terminal having a high potential. Klinger is silent on implementational details of the sampling circuit, but it is common practice of input a level to the data input and evidenced by Klinger (e.g., Figure 1a), as detailed supra.

Regarding claim 4, Klinger also discloses a general-purpose input/output (GPIO) controller (e.g., col. 6, lines 3-6).

Regarding claim 5, Klinger also discloses an integrated drive electronic (IDE) interface controller (e.g., col. 1, lines 30-36).

3. *Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klinger as applied in claim 6 above, in view of common digital design techniques, as evidenced by Rackley.*

Klinger discloses a D-type flip-flop having a clear terminal and a data input terminal such that said clear terminal couples with a system reset terminal (e.g., col. 6, lines 41-47). Klinger is expressly silent about the implementational details of using the triggering terminal of a D flip flop; however the Examiner takes Official Notice that it is widely known and practiced to use the clock input of a flip flop to sense signal variation. This is evidenced by Rackley who describes precisely this (e.g., Figure 1a). It would have been obvious to combine common digital design techniques with Klinger because the requirements of Klinger's sampling of a floating line, the details of which are expressly not disclosed, are commonly, simply, and advantageously solved by the well known technique of using a clock input on a flip flop. Therefore it would have been obvious to one of ordinary skill in the art to combine common practice with Klinger to obtain the claimed invention.

Response to Arguments

Applicant's arguments filed 1/12/05 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that Klinger does not disclose "that the D flip-flop is reset by the system reset" and that to the contrary, "Klinger states that the D-latch (one example of the sampling circuit 41) having its own reset control (column 6, line 45) and the reset control signal is independent from the main reset signal (column 6, lines 32-34). Klinger does not suggest the reset control signal of the sampling circuit 41 (or D-latch) have any relationship to the system reset, further, the reset control signal is independent form the main reset signal, which is a signal obtained by delay the system reset" (p. 2).

However, the only support for the distinction is the recitation of "a system reset". The Examiner finds that the particular reset of Klinger is resetting a "system". In this regard, the relationship between Klinger's reset and a "main reset signal" is immaterial in this determination because any distinction of a reset or of a system external to the claimed apparatus to which the reset is associated is wholly lacking in the claims.

Even if one were to afford a distinction of the claimed "system reset" as a particular reset of the (unrecited) motherboard, from context one finds that the reset is, in fact, associated with the main (i.e., motherboard) reset signal. Specifically, continuing from the Klinger citation used by the Applicant, Klinger teaches that "sampling circuit 41 includes logic elements, such as latches and control circuitry for providing the internal reset and sampling control from the main reset pulse on lead 42 which is transmitted to all parts of the machine" (col. 6, lines 34-38). Klinger's reset may not be a direct electrical connection to the motherboard reset; however it is a direct result of its assertion and can broadly be considered a motherboard-initiated reset

operation. Thus, the Examiner concludes that even were a distinct motherboard reset signal clearly established in the claims in distinction to the reset of Klinger, Klinger's reset is nonetheless associated therewith, save only in the narrowest sense.

Applicant further argues that "Klinger does not specify to use the system reset as the reset control signal of the sampling circuit"; however, as treated supra even were this an issue, we find that Klinger specifies precisely this.

Regarding claims 7 and 15, Applicant argues as treated supra.

Thus Examiner maintains the rejection made in the previous Office Action.

Continued Examination Under 37 CFR 1.114

All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100